Intel Compiler Optimization Guide

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Using the Intel compiler as a performance optimization and characterization tool*CP2K Tutorial: 1.3 CP2K installation, manual compilation with Intel compiler in Ubuntu (popt)* ~~Horizon Zero Dawn Optimization Guide~~ ~~The Complete Cemu Install Guide | Maximum Performance Setup~~ **Leveraging Compiler Optimization Reports**

OpenMP offload optimization guide: beyond kernels -Lessons learned in QMCPACK

Intel Compiler and VTune Performance Profiling Tool~~Intel Compilers Overview Scalable Performance for Intel Processors~~ ~~Compiler Optimization~~ **Performance Tuning on KNL with Intel Parallel Studio XE 2017 Cluster Edition** ~~CppCon 2017: Carl Cook “When a Microsecond Is an Eternity: High Performance Trading Systems in C++”~~ **Enterprise-scale machine translation with Spence Green, CEO of Lilt**

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Advanced CPU Designs: Crash Course Computer Science #94. Assembly Language \u0026 Computer Architecture

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Algorithmic and microarchitecture optimizations of C++ applications - Alexander Maslennikov*Performance: SIMD, Vectorization and Performance Tuning | James Reinders, former Intel Director* **Intel Compiler Optimization Guide**

Intel shipped a big update to their open-source Intel Graphics Compiler "IGC" that is used currently by their Windows driver, their Linux compute stack, and potentially their Linux graphics drivers ...

Intel Graphics Compiler 1.0.7683 Ships With Many Changes

Intel has been making noise in virtually all segments of the storage market as of late. A few weeks back, we took a look at the Optane Memory H20, which combines 3DXpoint media with traditional ...

Intel SSD D7-P5510 Review: Ultra-Fast PCIe 4 Enterprise Storage

When I tell people I’m a search engine optimization (SEO) specialist, I see their eyes glaze over. I often resort to a short response of, “I get companies to show up at the top of Google.” We all know ...

The Importance of SEO to Your Vacation Rental Website and Marketing Strategy

Intel appears to have changed just that with their newest Intel ... a metal VESA adapter plate to install the NUC 11 Pro on the back of a monitor, Quick Start Guide and the power brick. Perhaps just a ...

Intel NUC Pro Kit NUC11TNKV7 Review - Intel Moves to the Best in Sabrent Storage

Industry veteran Shlomit Weiss is returning to Intel to lead the company's full range of chip development and design—the entire CPU silicon gamut, in other words. Weiss brings with her over ...

Intel Recruits Revered Skylake Architect Shlomit Weiss To Lead Client CPU Development

While Clear Linux is certainly not the first distro developed by a tech heavyweight, it's a rare when a private company releases a distro with no direct commercial application. It's an experiment to ...

Clear Linux* Delivers a Lucid if Limited Vision of Desktop Linux

Intellimize, a startup leveraging AI to personalize websites for unique visitors, has raised $30 million in a venture capital round.

Intellimize raises $30M to optimize websites with AI

Inside every modern CPU since the Intel Pentium fdiv bug, assembly instructions aren’t a one-to-one mapping to what the CPU actually does. Inside the CPU, there is a decoder that turns assembly ...

34C3: Hacking Into A CPU’s Microcode

Quantum computers are beginning to emerge in many industry and research labs. But what are qubits? And are the challenges ahead to control the quantum properties ...

What is Quantum Computing?

It appears that Intel's Xe-HPG DG2 gaming GPU announcement ... (EUs), writing that there was still "lots of game and driver optimization work ahead." There was also a tweet from reliable leaker ...

Intel hints at imminent Xe-HPG DG2 gaming GPU reveal
While edge computing has seen an exponential growth in the last few years, developers are experiencing issues in implementing AI and edge software solutions. Intel DevCloud for the Edge addresses ...

Enabling telemetry for custom models in Intel DevCloud for the Edge
Last July, I took note when Intel released the Neural Compute Stick. It looked like an oversized USB stick, and acted as an accelerator for local AI applications, especially machine vision.

AI On Raspberry Pi With The Intel Neural Compute Stick
On our Test Bench today is the newest Intel SSD Optane P5800X PCIe 4.0 NVMe SSD and we must say that we are pretty impressed. In fact, I am left with a lingering question as to whether this level of ...

Intel Optane DC P5800X PCIe 4 NVME SSD Review - SSD Perfection Via Throughput, IOPS and Latency
"Intel Bridge Technology is a run-time post compiler to enable applications that are not compiled to run natively on x86-based devices—such as Android-based mobile applications—to run on those ...

Windows 11 will let you run Android apps directly on the desktop
Intel says Bridge is a runtime post-compiler that allows applications that were originally designed for a variety of different hardware platforms to run natively on x86 devices. The company points ...

Intel's Bridge technology will allow Android apps to run natively on Windows 11
Editors' Note: Intel and Microsoft have provided a statement to Tom's Guide with further clarification ... "Intel Bridge Technology is a runtime post-compiler that enables applications to run ...

Windows 11 will run Android apps — here's how
At Microsoft's Windows 11 unveil event Thursday (June 24), the software giant announced that PC apps will not be alone on this new OS. Windows 11 will run Android apps — but that does not mean ...

Windows 11 Android apps — be prepared for disappointment
Intel has plotted out its strategy to re-take the CPU crown from AMD, and APC dives in deep to reveal just what tricks and tech Team Blue has in store for us. Plus, the hot new Nvidia RTX 3070 Ti ...

APC's August issue is on sale now!
With the best RAM for gaming, you can ensure that your CPU and graphics card are running optimally. It's the easiest and swiftest upgrade for your rig, and seeing as dropping the best graphics ...

The best RAM for gaming in 2021
We've been hotly anticipating the arrival of Intel's official desktop gaming graphics cards for a while now, and we're pretty sure they will be launching sometime this year. But the Blue ...

Intel® Xeon PhiTM Coprocessor Architecture and Tools: The Guide for Application Developers provides developers a comprehensive introduction and in-depth look at the Intel Xeon Phi coprocessor architecture and the corresponding parallel data structure tools and algorithms used in the various technical computing applications for which it is suitable. It also examines the source code-level optimizations that can be performed to exploit the powerful features of the processor. Xeon Phi is at the heart of world's fastest commercial supercomputer, which thanks to the massively parallel computing capabilities of Intel Xeon Phi processors coupled with Xeon Phi coprocessors attained 33.86 teraflops of benchmark performance in 2013. Extracting such stellar performance in real-world applications requires a sophisticated understanding of the complex interaction among hardware components, Xeon Phi cores, and the applications running on them. In this book, Rezaur Rahman, an Intel leader in the development of the Xeon Phi coprocessor and the optimization of its applications, presents and details all the features of Xeon Phi core design that are relevant to the practice of application developers, such as its vector units, hardware multithreading, cache hierarchy, and host-to-coprocessor communication channels. Building on this foundation, he shows developers how to solve real-world technical computing problems by selecting, deploying, and optimizing the available algorithms and data structure alternatives matching Xeon Phi's hardware characteristics. From Rahman's practical descriptions and extensive code examples, the reader will gain a working knowledge of the Xeon Phi vector instruction set and the Xeon Phi microarchitecture whereby cores execute 512-bit instruction streams in parallel.

Coding and testing are often considered separate areas of expertise. In this comprehensive guide, author and Java expert Scott Oaks takes the approach that anyone who works with Java should be equally adept at understanding how code behaves in the JVM, as well as the tunings likely to help its performance. You'll gain in-depth knowledge of Java application performance, using the Java Virtual Machine (JVM) and the Java platform, including the language and API. Developers and performance engineers alike will learn a variety of features, tools, and processes for improving the way Java 7 and 8 applications perform. Apply four principles for obtaining the best results from performance testing Use JDK tools to collect data on how a Java application is performing Understand the advantages and disadvantages of using a JIT compiler Tune JVM garbage collectors to affect programs as little as possible Use techniques to manage heap memory and JVM native memory Maximize Java threading and synchronization performance features Tackle performance issues in Java EE and Java SE APIs Improve Java-driven database application performance

The second instance of the international summer school on Generative and Transformational Techniques in Software Engineering (GTTSE 2007) was held in Braga, Portugal, during July 2-7, 2007. This volume contains an augmented selection of the material presented at the school, including full tutorials, short tutorials, and contributions to the participants workshop. The GTTSE summer school series brings together PhD students, lecturers, technology presenters, as well as other researchers and practitioners who are interested in the generation and the transformation of programs, data, models, metamodels, documentation, and entire software systems. This concerns many areas of software engineering: software reverse and re-engineering, model-driven engineering, automated software engineering, generic language technology, to name a few. These areas di?er with regard to the speci?c sorts of metamodels (or grammars, schemas, formats etc.) that underlie the involved artifacts, and with regard to the speci?c techniques that are employed for the generation and the transformation of the artifacts. The ?rst instance of the school was held in 2005 and its proceedings appeared as volume 4143 in the LNCS series.

Authors Jim Jeffers and James Reinders spent two years helping educate customers about the prototype and pre-production hardware before Intel introduced the first Intel Xeon Phi coprocessor. They have distilled their own experiences coupled with insights from many expert customers, Intel Field Engineers, Application Engineers and Technical Consulting Engineers, to create this authoritative first book on the essentials of programming for this new architecture and these new products. This book is useful even before you ever touch a system with an Intel Xeon Phi coprocessor. To ensure that your applications run at maximum efficiency, the authors emphasize key techniques for programming any modern parallel computing system whether based on Intel Xeon processors, Intel Xeon Phi coprocessors, or other high performance microprocessors. Applying these techniques will generally increase your program performance on any system, and better prepare you for Intel Xeon Phi coprocessors and the Intel MIC architecture. A practical guide to the essentials of the Intel Xeon Phi coprocessor Presents best practices for portable, high-performance computing and a familiar and proven threaded, scalar-vector programming model Includes simple but informative code examples that explain the unique aspects of this new highly parallel and high performance computational product Covers wide vectors, many cores, many threads and high bandwidth cache/memory architecture

A Guide to RISC Microprocessors provides a comprehensive coverage of every major RISC microprocessor family. Independent reviewers with extensive technical backgrounds offer a critical perspective in exploring the strengths and weaknesses of all the different microprocessors on the market. This book is organized into seven sections and comprised of 35 chapters. The discussion begins with an overview of RISC architecture intended to help readers understand the technical details and the significance of the new chips, along with instruction set design and design issues for next-generation processors. The chapters that follow focus on the SPARC architecture, SPARC chips developed by Cypress Semiconductor in collaboration with Sun, and Cypress's introduction of redesigned cache and memory management support chips for the SPARC processor. Other chapters focus on Bipolar Integrated Technology's ECL SPARC implementation, embedded SPARC processors by LSI Logic and Fujitsu, the MIPS processor, Motorola 88000 RISC chip set, Intel 860 and 960 microprocessors, and AMD 29000 RISC microprocessor family. This book is a valuable resource for consumers interested in RISC microprocessors.

Optimizing HPC Applications with Intel® Cluster Tools takes the reader on a tour of the fast-growing area of high performance computing and the optimization of hybrid programs. These programs typically combine distributed memory and shared memory programming models and use the Message Passing Interface (MPI) and OpenMP for multi-threading to achieve the ultimate goal of high performance at low power consumption on enterprise-class workstations and compute clusters. The book focuses on optimization for clusters consisting of the Intel® Xeon processor, but the optimization methodologies also apply to the Intel® Xeon Phi™ coprocessor and heterogeneous clusters mixing both architectures. Besides the tutorial and reference content, the authors address and refute many myths and misconceptions surrounding the topic. The text is augmented and enriched by descriptions of real-life situations.

This book is an all-in-one source of information for programming the Second-Generation Intel Xeon Phi product family also called Knights Landing. The authors provide detailed and timely Knights Landingspecific details, programming advice, and real-world examples. The authors distill their years of Xeon Phi programming experience coupled with insights from many expert customers — Intel Field Engineers, Application Engineers, and Technical Consulting Engineers — to create this authoritative book on the essentials of programming for Intel Xeon Phi products. Intel® Xeon PhiTM Processor High-Performance Programming is useful even before you ever program a system with an Intel Xeon Phi processor. To help ensure that your applications run at maximum efficiency, the authors emphasize key techniques for programming any modern parallel computing system whether based on Intel Xeon processors, Intel Xeon Phi processors, or other high-performance microprocessors. Applying these techniques will generally increase your program performance on any system and prepare you better for Intel Xeon Phi processors. A practical guide to the essentials for programming Intel Xeon Phi processors Definitive coverage of the Knights Landing architecture Presents best practices for portable, high-performance computing and a familiar and proven threads and vectors programming model Includes real world code examples that highlight usages of the unique aspects of this new highly parallel and high-performance computational product Covers use of MCDRAM, AVX-512, Intel® Omni-Path fabric, many-cores (up to 72), and many threads (4 per core) Covers software developer tools, libraries and programming models Covers using Knights Landing as a processor and a coprocessor

This guide provides a comprehensive overview of High Performance Computing (HPC) to equip students with a full skill set including cluster setup, network selection, and a background of supercomputing

competitions. It covers the system, architecture, evaluating approaches, and other practical supercomputing techniques. As the world’s largest supercomputing hackathon, the ASC Student Supercomputer Challenge has attracted a growing number of new talent to supercomputing and has greatly promoted communications in the global HPC community. Enclosed in this book, readers will also find how to analyze and optimize supercomputing systems and applications in real science and engineering cases.

This book constitutes the refereed proceedings of the 10th International Conference on Cryptology in India, INDOCRYPT 2009, held in New Dehli, India, in December 2009. The 28 revised full papers were carefully reviewed and selected from 104 submissions. The papers are organized in topical sections on post-quantum cryptology, key agreement protocols, side channel attacks, symmetric cryptology, hash functions, number theoretic cryptology, lightweight cryptology, signature protocols, and multiparty computation.

Learn how to accelerate C++ programs using data parallelism. This open access book enables C++ programmers to be at the forefront of this exciting and important new development that is helping to push computing to new levels. It is full of practical advice, detailed explanations, and code examples to illustrate key topics. Data parallelism in C++ enables access to parallel resources in a modern heterogeneous system, freeing you from being locked into any particular computing device. Now a single C++ application can use any combination of devices—including GPUs, CPUs, FPGAs and AI ASICs—that are suitable to the problems at hand. This book begins by introducing data parallelism and foundational topics for effective use of the SYCL standard from the Khronos Group and Data Parallel C++ (DPC++), the open source compiler used in this book. Later chapters cover advanced topics including error handling, hardware-specific programming, communication and synchronization, and memory model considerations. Data Parallel C++ provides you with everything needed to use SYCL for programming heterogeneous systems. What You'll Learn Accelerate C++ programs using data-parallel programming Target multiple device types (e.g. CPU, GPU, FPGA) Use SYCL and SYCL compilers Connect with computing’s heterogeneous future via Intel’s oneAPI initiative Who This Book Is For Those new data-parallel programming and computer programmers interested in data-parallel programming using C++.